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10/708,101	02/09/2004	Yao Tung Yen	PS-108	2100

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,101	YEN, YAO TUNG	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-8,19 and 20* is/are allowed.

6)☒ Claim(s) *9-17* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0204//09 Feb 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 9 is objected to because of the following informalities:

In Claim 9, line 27: "to" (following the word "connect") should be deleted.

Appropriate correction is required.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Hashimoto (US 6,483,718 B2) Moshayedi (US 2004/0212071 A1)

Isaak (US 6,472,735 B2)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 9-11, 13, 14 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto.

As to Claim 9, Hashimoto discloses, in Figs. 1 and 2: a top BGA device 10 (i.e., middle device 10) having an array of first contacts 14 on a lower surface; a bottom BGA device 10 (i.e., the bottommost device 10) having an array of first contacts 14 on a lower surface; an intermediate adapter card 20 (i.e., middle card 20) having a top

surface facing the lower surface of top BGA device 1, and a lower surface facing the bottom BGA device 10; a first array of metal contacts 32 on the top surface of intermediate adapter card 20 for electrically contacting the array of first contacts 14 of top BGA device 10; intermediate metal traces 30 on intermediate adapter card 20 that connect to the first array of metal contacts 32; peripheral connectors 40, electrically connected to intermediate traces 30, "disposed around edges" (which is broadly interpreted by the Examiner as proximate the edges, i.e., at the peripheral edge of the card, as in Figs. 15A,B and 16; not necessarily wrapped around or covering the vertical side edges) of intermediate adapter card 20; a bottom adapter card 20 having a top surface facing the lower surface of the bottom BGA device 10, and a lower surface facing a mounting board (not shown in Fig. 1 but disclosed in col.10: 1-7); a second array of metal contacts 32 on the top surface of the bottom adapter card 20 for electrically contacting the array of second contacts 14 of the bottom BGA device 10; peripheral pads 41 on the top surface of bottom adapter card 20, for contacting the peripheral connectors 40 of the intermediate adapter card 20; bottom metal traces 30 on the bottom adapter card 20 that connect the second array of metal contacts 32 to the peripheral pads 41 (col.8: 46-48); final bonding pads (i.e., metallization 52 of projections 50; col.9: 45-58) on the bottom adapter card 20 and electrically connected to the bottom metal traces 30, for soldering to the mounting board (using the same solder material (44, 54) that fills the projections and that may be used to interconnect adapter boards 20 to one another, as in one disclosed embodiment; col.8: 3-5 and 14-19, col.9: 65-67 and col.10: 1-7).

As to Claim 10, Hashimoto further discloses the bottom metal traces 30 on the bottom adapter card 20 are formed on the top surface of the bottom adapter card (Figs. 1 and 2).

As to Claim 11, Hashimoto further discloses vias 24 through the bottom adapter card 20 for connecting the bottom metal traces 30 on the top surface of the bottom adapter card 20 to the final bonding pads 52 on the lower surface of the bottom adapter card 20 (Fig. 1; col.9: 35-44).

As to Claim 13, Hashimoto further discloses the intermediate metal traces 30 on the intermediate adapter card 20 are formed on the top surface of the intermediate adapter card 20 (Fig. 1).

As to Claim 14, Hashimoto further discloses the mounting board is a motherboard (col.1: 9-22; col.10: 1-4).

As to Claim 17, Hashimoto further discloses the peripheral connectors are lead frame pins 40 (col.7: 35-53).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto.

I. Hashimoto is silent as to how the peripheral connectors 40 of intermediate adapter card 20 are connected to peripheral pads 41 of the bottom adapter card 20 to make electrical connections.

II. Hashimoto teaches that when convexities 46 of peripheral connectors 40 on one adapter 20 are connected to the concavities 48 on the next lower adapter 20, without penetrating the concavities 48, then the connection is effected by the conducting material 44 that fills the concavities (col.8: 14-19), wherein the conducting material 44 is solder (col.8: 3-5). Hashimoto further teaches that peripheral pad 41 on the bottom adapter card 20 is a land (col.8: 36-43, hence, not a concavity into which connector 40 may penetrate.

III. Since solder paste 44 is used to fill peripheral connectors 40 and since peripheral pad 41 is a land and not a concavity into which connector 40 may penetrate, then using the same solder paste material as conducting material 44 in order to effect the surface mount connection of the metallization of connector 40 onto peripheral pad 41 would have been readily recognized in the pertinent art of Hashimoto since he teaches a similar solder connection between the upper adapters 20, as discussed, above.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to establish the disclosed connection between the peripheral connectors 40 of the intermediate adapter card 20 and the peripheral pads 41 of the bottom adapter card 20 by use of the disclosed solder paste material 44.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto in view of Moshayedi.

I. Hashimoto discloses the top and bottom BGA devices 10 are each memory (i.e., integrated circuit) chips (col.9: 7-17) and at least partially packaged (col.5: 28-31) but does not positively indicate whether they are bare chips or packaged chips.

II. Moshayedi discloses a stack of chips wherein the chips are "generally planar encapsulated integrated circuits of types well-known in the art" (paragraph [0045]).

III. Since both Hashimoto and Moshayedi are in the art of stacked semiconductor devices, then the use of packaged IC chips for an application, taught in Moshayedi et al., wherein the packaging provides protection against ambient moisture and contaminants, would have been readily recognized as chips for use in the pertinent stacked assembly art of Hashimoto.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide packaged IC memory chips in the stacked assembly of Hashimoto, as taught by Moshayedi et al., in order to provide the memory chips with protection against ambient moisture and contaminants, thus enhancing the operational reliability of the stacked assembly.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto in view of Moshayedi as applied to Claim 15, above, and further in view of Isaak.

I. Hashimoto discloses that the array of first contacts 14 (corresponding to electrodes 12) of top BGA device 10 (memory chip), and the array of second contacts

14 (corresponding to electrodes 12) of bottom BGA device 10 (memory chip), each may be formed in variety of array configurations on various regions of the active surface; e.g., the extremities (i.e. periphery), the central portion, on a pair of opposing sides or on all four sides (col.5: 23-33).

II. Hashimoto does not disclose a 4 x 4 contact array.

III. Isaak discloses a stacked semiconductor chip assembly including BGA chips 70 having contact arrays 82 of at least 4 rows x 4 columns (Figs. 2 and 4; col.11: 29-33), with each contact 82 in the array connected to a peripheral pad 26 by metal traces 28 between the array pads 24 and peripheral pads 26 on adapter card 12 (Fig. 4; col.7: 41-43), in order to accommodate the required I/O and other signals to/from chips 70.

IV. Since both Hashimoto and Isaak are in the art of stacked chip assembly art and Hashimoto discloses various chip array configurations wherein the chip contacts are each connected to corresponding contacts on an adapter card and connected by metal traces to peripheral pads and connectors on the adapter card, and since Isaak also teaches such a stacked structure and chip connection wiring but with chips having at least a 4 x 4 column/row array, then such 4 x 4 array chips would have been readily recognized for use in the pertinent art of Hashimoto in order to meet the chip type requirements for an application.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the adapter card wiring of Hashimoto in order to accommodate any chips with functionality required by an application, wherein the chips have a contact array of at least 4 x 4, as taught in the stacked assembly of Isaak.

Allowable Subject Matter

9. Claims 1-8 and 19-20 have been allowed.

10. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 1-8, patentability resides in **the combination of** *lead frame pins that wrap around edges of the intermediate adapter card from the first surface to below a second surface of the intermediate adapter card* **and** *the claimed peripheral pads of the bottom adapter card disposed to make electrical contact with the lead frame pins from the intermediate adapter card*, in combination with the other limitations of base Claim 1.

As to Claim 18, patentability resides in a molding under the lower surface of the intermediate adapter card for shaping the peripheral connectors into a U shape, in combination with the other limitations of the claim.

As to Claims 19-20, patentability resides in the **combination of** *lead frame means for wrapping around edges of the intermediate adapter card from the first surface to below a second surface of the intermediate adapter card means* **and** *the claimed peripheral pads of the bottom adapter card means, for making electrical contact with the lead frame means from the intermediate adapter card means*, in combination with the other limitations of base Claim 19.

12. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Chung (US 6,376,769 B1) discloses, in Fig. 16: a top BGA device 320-2 with first array of contacts 324 on a lower surface; a bottom BGA device 320-1 having an array of second contacts on a lower surface; an intermediate adapter card 310-2 having a top surface facing the lower surface of the top BGA device 320-2, and a lower surface facing the bottom BGA device 320-1; a first array of metal contacts 312 on the top surface of intermediated adapter card 310-2 for electrically contacting the array of first contacts 324 of top BGA device 320-2; intermediate metal traces 313 on intermediate adapter card 310-2 that connect to the first array of metal contacts 312 (col.18: 58-61); peripheral connectors 315, electrically connected to the intermediate metal traces 313, "disposed around the edges" (which may be broadly interpreted as proximate the edges, i.e., at the peripheral edge of the card, as in Figs. 15A,B and 16; not necessarily wrapped around or covering the vertical side edges) of intermediate adapter card 310-2 (Figs. 15A,B; col.18: 58-61); a bottom adapter card 310-1 having a top surface facing the lower surface of bottom BGA device 320-1, and a lower surface facing a mounting board 340 (col.20: 12-18); a second array of metal contacts 312 on the top surface of

the bottom adapter card 310-1 for electrically contacting the array of second contacts 324 of the bottom BGA device 320-1; peripheral pads 315 on the top surface of the bottom adapter card 310-1, for electrically **connecting** to the peripheral connectors 315 of the intermediate card 310-2, the electrical connection occurring through vias 335 of an interposer portion 330-1 (note that peripheral pads 315 on the top surface of the bottom adapter card 310-1 are **NOT** "for **contacting** the peripheral connectors;" rather, the peripheral pads 315 on the top surface of the bottom adapter card 310-1 are for **contacting the via pads on the bottom surface of the intervening interposer portion 330-1**); bottom metal traces 313 on the (top surface of) bottom adapter card 310-1 that connect to the second array of metal contacts 312 to peripheral pads 315; final bonding pads (corresponding to bumps 334) on the bottom adapter card 310-1 and electrically connected to the bottom metal traces 313, for soldering to mounting board 334 (col.20: 24-27).

b) Senba et al. (US 6,188,127 B1) discloses a stacked semiconductor device structure (Figs. 4D,E) with peripheral connectors 7 that pass signals among the adapter cards 2. Senba et al. further discloses an embodiment with additional conductive portions 20 wrapped around the edges of the adapter cards 2, wherein the conductive portions 20 are connected to ground and act as a kind of Faraday cage preventing the chips from electromagnetically interfering with one another (col.7: 59-67).

c) Jeong et al. (US 6,861,737 B1) discloses a chip wire-bonded to an adapter card and lead frame pins that wrap around edges of the adapter card from the first

surface to below a second surface of the adapter card, and the stacking of the adapter cards (e.g., Figs. 7 & 10 and Figs. 4F & 8).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
March 19, 2006